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Modeling and analysis of temperature and thermomechanical stress distributions in a multi-chip electronic module

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Abstract: **A mathematical thermomechanical model of a multi-chip electronic module (MEM) containing three silicon dies of high-power transistors fixed with a conductive adhesive on a copper plate placed on a radiator is considered in the form of a system of equations of thermal conductivity and thermoelasticity with specified boundary conditions. As a result of computational studies of the model in the COMSOL Multiphysics software environment, distributions of temperature and thermomechanical stresses in the MEM structural elements were obtained depending on the heating power, the thickness of the adhesive and the size of the model defect in the contact connection of one of the MEM crystals with a copper plate in the form of voids in the adhesive layer. It is shown that voids in the adhesive layer lead to a sharply non-uniform temperature distribution over the crystal area and thermomechanical shear stresses in the contact layer that exceed the maximum permissible values for the adhesive. It has been established that thermomechanical stresses decrease with increasing thickness of the adhesive layer and increase with increasing size of the defect(voids) in this layer. The simulation results are in good agreement with the results of measuring the thermal impedance of power transistor crystals using the modulation method, which indicates the correctness and adequacy of the developed model.**

Keywords: **multi-chip electronic module, thermomechanical model, contact connection, defect, temperature distribution, thermomechanical stress, thermal resistance, modulation method**

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1. INTRODUCTION

When power is dissipated in the active elements of multi-chip electronic modules (MEMs), which are several semiconductor crystals mounted on a common thermally conductive substrate (for

example, power modules of high-power bipolar, MOSFET or IGBT transistors on a copper plate), the crystals and structural elements of the MEM heat up , at the same time, due to the difference in the coefficients of thermal expansion of the materials of the MEM construction, thermomechanical stresses and deformations arise in them. Critical values of thermal overheating and thermomechanical stresses are the main causes of failures of MEM elements. These factors lead to accelerated degradation of the contact connections of the crystals with the substrate and, as a consequence, to an increase in thermal resistance and deterioration of heat dissipation, which in turn leads to a further increase in temperature, mechanical stress and deformation of MEM structural elements, which ultimately leads to deterioration operational characteristics and failures of MEM [1–3].

One of the most important factors in MEM reliability is the quality of the adhesive bond between the chip and the substrate. The presence of voids in the adhesive layer between the crystal and the substrate in MEMs is one of the main reasons for the accelerated degradation of contact connections as a result of thermomechanical deformations and reduced service life of devices [4]. The study of these processes requires taking into account many factors and stimulates the development of new thermoelectric and thermomechanical models of MEMs. Recently, problems associated with heating of power and microwave MEMs during operation have been solved using computer modeling methods in various software environments - ABAQUS, ANSYS Workbench, COMSOL Multiphysics [5–7], however, the influence of defects in the area of contact of the crystal with the substrate in these models not considered. The purpose of this work is to create a thermomechanical model and, with its help, carry out studies of thermomechanical stresses that arise in the structural elements of the MEM depending on the parameters of the defect.

The object of study was a multi-chip power electronic module consisting of three crystals of silicon high-power bipolar transistors (**Fig. 1**). The crystals were fixed to a copper substrate using a conductive adhesive, which was placed on a radiator through a layer of thermal paste. To assess the influence of the quality of the contact layer on the distribution of temperature and thermomechanical stresses in the MEM design, a defect in the form of voids or incomplete filling of the contact connection between the crystal and the substrate with adhesive was artificially introduced into the contact layer of one of the crystals.

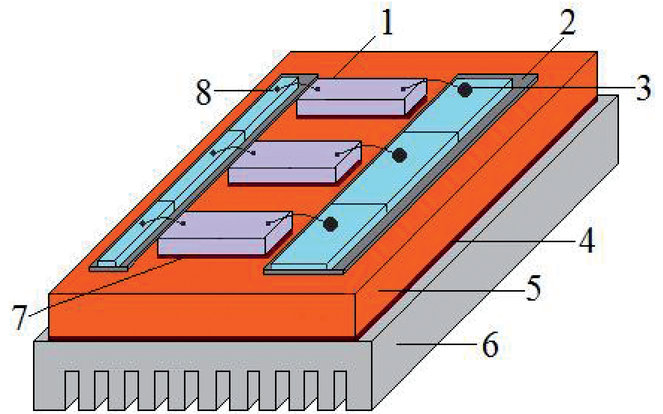

Fig. 1. *MEM design: 1—dies; 2—dielectric; 3—emitter terminal; 4—thermal paste; 5—copper substrate; 6—radiator; 7—adhesive; 8—base pin.*

2. DESCRIPTION OF THE THERMOMECHANICAL MODEL

Calculated temperature and thermal deformation studies of the MEM were carried out for a simplified model structure, the geometry of which is presented in **Fig. 2**. In the area of the adhesive connection of the third crystal with the substrate, a defect was modeled, which was characterized by the coefficient of the relative size of the defect $K_S = S_D - S_0$, where S_D, S_0 are the areas of the defect area and the lower surface of the crystal, respectively.

The temperature field $T_i(x,y,z)$ in the structure of a multicrystal system and the

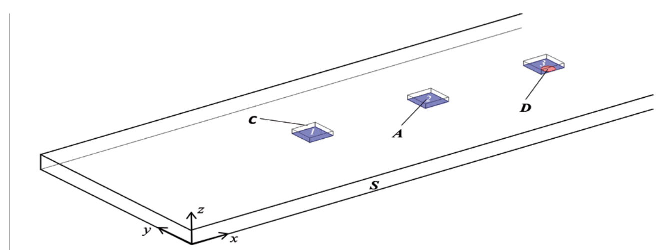

Fig. 2. *Geometry of the MEM calculation model: C — silicon crystal; A — adhesive layer; D — defect; S — copper substrate.*

deformation movements of its layers $\vec{u}_i(x,y,z,t)$ are determined from the joint solution of the equations of thermoelasticity and thermal conductivity [8]:

$$\mu_i \nabla^2 \vec{u}_i + (\lambda_i + \mu_i)\nabla(\nabla \vec{u}_i) - \\ -(3\lambda_i + 2\mu_i)\alpha_i \nabla (T_i - T_0) = 0, \;\; \mathrm{i} = 1,...,8, \quad (1)$$

$$\nabla\left(k_i(T_i)\nabla T_i\right) = 0, \quad (2)$$

where T_0 – is the ambient temperature; $\lambda_i = \frac{\nu_i E_i}{(1+\nu_i)(1-2\nu_i)}$, $\mu_i = \frac{E_i}{2(1+\nu_i)}$ – Lamé coefficients; $E_i(T_i)$, $\nu_i(T_i)$, $\alpha_i(T_i)$ – elastic modulus, Poisson's ratio and coefficient of thermal expansion of structure materials; $k_i(T_i)$ – thermal conductivity coefficients of structure materials.

All external surfaces of MEM elements are considered free. The temperature of the bottom surface of the substrate base is assumed to be equal to the radiator temperature T_r. The power density is set on the top surfaces of each of the three MEM semiconductor chips

$$q = -\lambda_i(T_i)\left.\frac{\partial T_i}{\partial z}\right|_{z=h} = \frac{W}{S_{ar}}, \quad (3)$$

where W – is the thermal power dissipated by the crystal, S_{ar} is the area of the active region of the crystal; $h = \sum_{k=1}^{3} h_k$ – height of the MEM, h_k thickness of the k-th layer of the MEM structure. All external surfaces S_i of the MEM structure are under conditions of natural heat exchange:

$$\lambda_i T_{i_z}\big|_{S_i} + \alpha_n\left(T_0 - T_i\big|_{S_i}\right) = 0, \quad (4)$$

where α_n – is the heat transfer coefficient by natural convection, the value of which lies in the range of 5÷25 $W/(m^2 \cdot K)$ and is a model parameter. During the calculation process, it is refined by an iterative method according to experimental data on the heating temperature of the selected structural element of the MEM model. Subsequently, in the presented calculation version, this temperature was the temperature of the *p-n* junction of the 3rd crystal.

3. SIMULATION RESULTS AND DISCUSSION

The solution to the model problem (1) – (4) was found using a numerical method. The developed program included access to the COMSOL Multiphysics software.

In the experimental model MEM model considered in this article, the dimensions of the copper plate were – 85×17×1.5 mm; and KT504 transistor crystals with dimensions 2×2×0.45 mm were used as silicon crystals. The adhesive used was XH9960-1 adhesive from NAMICS [9] with a thermal conductivity coefficient λ_A = 75 $W/m \cdot K$; the thickness of the adhesive layer during calculations varied within δ = 5÷50 μm; air voids with a thermal conductivity coefficient λ_A = 0.022 $W/m \cdot K$ were considered as a defect in the adhesive layer, and the coefficient of the relative size of the defect varied within the range K_S = 0.05÷0.2. The power dissipated by the crystals was W = 10 W, which is the maximum allowable power for this type of transistor.

Computational studies have shown that the maximum temperature in the structure is achieved on the upper surface of the 3rd crystal (z = 1.98 mm) in the region located above the center of the defect (z = 1.53 mm) (**Fig. 3**).

Analysis of the profiles shows that near the boundaries of the defect (voids) in the adhesive layer, the temperature gradient increases sharply, which in turn leads to a sharp increase in thermomechanical shear stresses (**Fig. 4**).

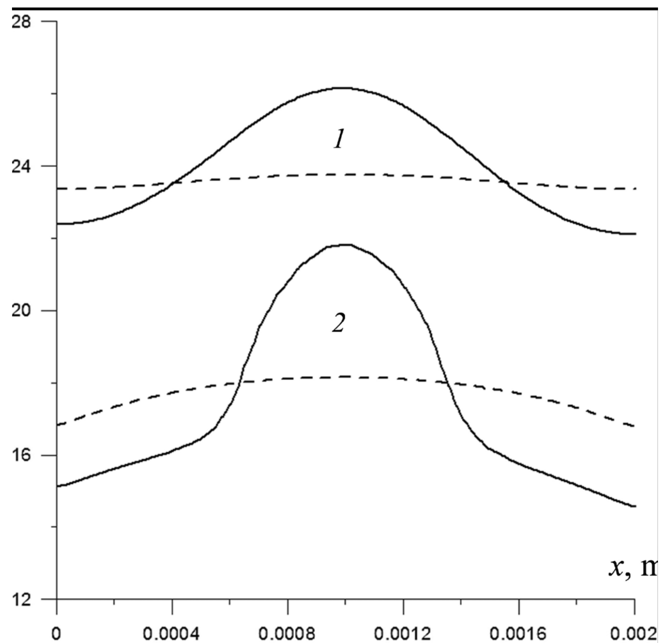

Fig. 3. *Temperature distribution on the upper (1) and lower (2) surfaces of crystals (along the symmetry axis of the crystal) with adhesive layer thickness δ = 30 μm and relative defect size K_S = 0.2: (solid line – crystal 3, dotted line – crystal 2).*

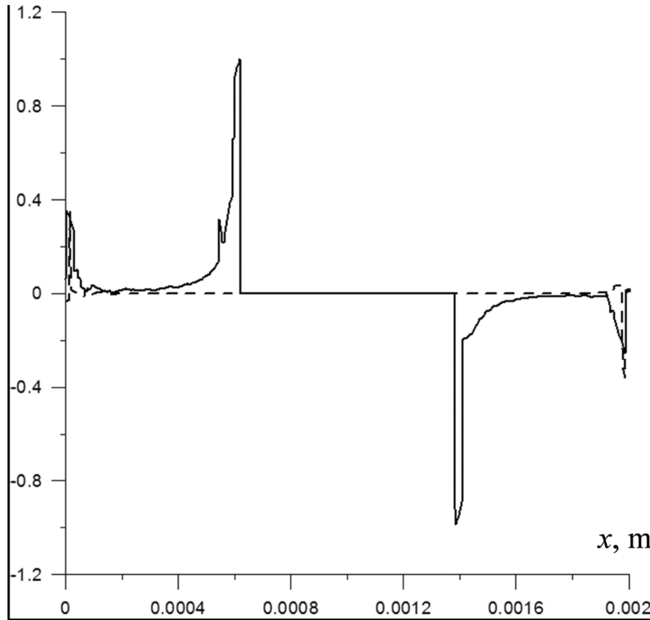

Fig. 4. *Distribution of thermomechanical shear stress in an adhesive layer with a defect at the boundary with crystal No. 3: z = 1.53 mm, K_S = 0.2, δ = 30 μm.*

The values of mechanical stress on the graph are indicated in relative units, reduced to the limiting value of shear stress for a given type of adhesive, equal to σ_{SC} = 13 MPa [9]. As can be seen from the presented dependence for a transistor with a defect in the contact connection, operating at the maximum permissible power, the shear stress near the boundaries of the defect reaches the limiting value of $\sigma_S/\sigma_{SC} \approx 1$, that is, the crystal can shift, followed by its separation from the substrate.

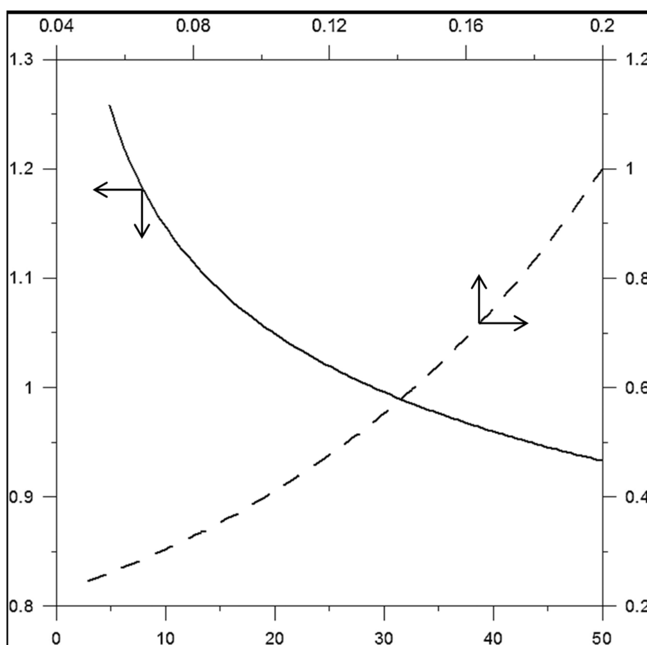

Fig. 5. *Dependence of thermomechanical shear stress on model parameters, σSC= 13 MPa.*

Fig. 5 presents the results of computational studies of the dependence of shear stress on the relative size of the defect K_S and on the thickness of the adhesive layer δ.

Analysis of the obtained results shows that thermomechanical shear stress decreases with increasing adhesive thickness. At values δ << 10 μm, a rapid increase in shear stress is observed. Thus, for the presented design variant of the structure, reducing the thickness of the adhesive layer by three times leads to an increase in the value of the shear stress to a value of 1.2 σ_{SC}. With increasing defect size K_S, the maximum value of thermomechanical shear stress increases, which, as already noted, leads to accelerated degradation of the contact joint. The results obtained using well-known models of destruction (degradation) of contact joints [10] make it possible to quantify the influence of the size of the defect (voids) in the adhesive layer on its reliability.

4. EXPERIMENTAL VERIFICATION OF SIMULATION RESULTS

To estimate the increase in crystal temperature ΔT_j (transistor junction temperature) when a given power is dissipated in them, the thermal resistance between the *p-n* junction of the transistor and the substrate on which the crystals were mounted was measured. According to the standards, the thermal resistance of the transistor R_{Tjc} relative to its body is determined by the increase in the temperature of the *p-n* junction of the transistor when unit thermal power is dissipated in it [11]:

$$R_{Tjc} = \frac{T_j - T_c}{P} = \frac{\Delta T_j}{P}, \quad (5)$$

where T_j is the junction temperature of the transistor; T_c is the fixed temperature of the case or substrate on which the crystal is mounted; P – power dissipated in the transistor.

Thermal resistance measurements were carried out using the modulation method [12], in which a sequence of heating current pulses with a constant repetition period and a duration varying according to a harmonic law was passed through each transistor. Such pulse-width modulation of the heating power caused a periodic change in the transition temperature of the transistors

$T_j(t)$, shifted in phase relative to the power $P(t)$ by a certain angle φ. By measuring the amplitude of the variable component of the transition temperature T_{j1} by changing the temperature-sensitive parameter (*T*SP), which linearly depends on T_j, and knowing the amplitude of the variable component of the dissipated power P_1, we can determine the modulus Z_T and phase φ of the thermal impedance at the modulation frequency ν:

$$Z_T = \frac{T_{j1}}{P_1}, \quad \varphi = arctg\frac{\operatorname{Im} T_j}{\operatorname{Re} T_j}, \qquad (6)$$

where Im T_j и Re T_j – imaginary and real Fourier transforms of the transition temperature at the modulation frequency ν.

The modulation method makes it possible to measure the components of thermal resistance determined by the design features of the object through which the heat flow propagates from the active region of the crystal to the substrate and further to the radiator and the environment [13]. To do this, the dependence of the module $Z_T(\nu)$, phase φ(ν) and the real part Re $Z_T(\nu)$ of the thermal impedance on the modulation frequency ν of the heating power is measured. These dependencies have features in the form of flat sections and inflection points, which are associated with the components of thermal resistance. To identify these features, Re $Z_T(\nu)$ is smoothed and subsequently differentiated by modulation frequency. Smoothing is carried out using spline interpolation of the Re $Z_T(\nu)$ dependence, and the derivative is calculated based on the calculation of linear regression coefficients at each point of the Re $Z_T(\nu)$ graph. The number of points for smoothing and derivative calculation is specified by the operator.

Thermal resistance components were measured using a hardware-software complex that implemented the modulation method [14]. The transistor was connected according to a common base circuit. The direct voltage at the emitter of the transistor at a measuring current of 10 mA was used as a TPP. The amplitude of the heating current pulses was set to 1000 mA, the pulse repetition period was 480 μs, and the heating power modulation frequency was varied in the range from 2 to 400 Hz. The results of measuring the frequency dependence of the real part Re $Z_T(\nu)$ of the thermal impedance for transistor No. 2 are presented in **Fig. 6.**

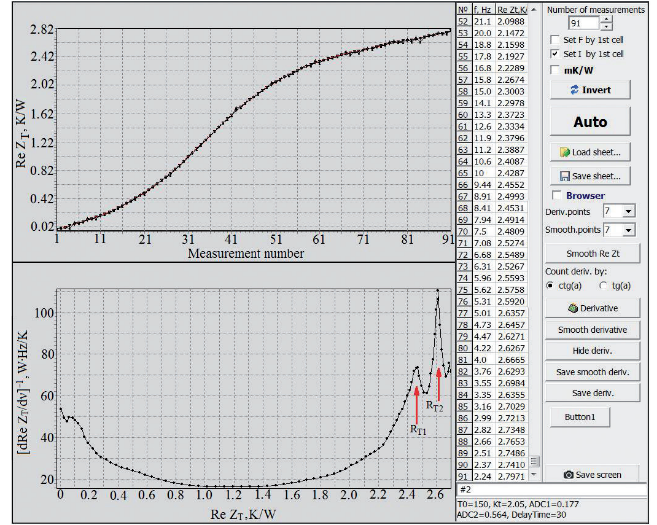

Fig. 6. *Frequency dependence of the real part of the thermal impedance (top) and the result of its processing (bottom).*

The upper graphic window shows the smoothed dependence Re $Z_T(\nu)$ with the number of points for smoothing set by the operator equal to 7. The lower window shows the dependence $[d(\operatorname{Re} Z_T)/d\nu]^{-1}$ as a function of the variable Re Z_T. The position of local maxima relative to the x-axis allows us to determine the components of thermal resistance R_T. The first maximum corresponds to the thermal resistance component R_{T1} "junction-substrate", the second maximum corresponds to the component R_{T2} "junction-radiator". The values of R_{T1} and R_{T2} for transistor No. 2 are 2.45 and 2.62 *K*/*W*, respectively. The measurement results of R_{T1} and R_{T2} for transistor No. 1 differ from the values for transistor No. 1 by no more than 3% and were not considered further. Similar measurements of the thermal resistance components, carried out for crystal No. 3 with a defect in mounting to the substrate, gave the values R_{T1} = 2.63 *K*/*W* and R_{T2} = 2.84 *K*/*W*. With 10 *W* of power dissipated in both transistors, the transition temperature increment ΔT_j relative to the substrate will be 24.5°C for the 2nd crystal, and 26.3°C for the 3rd crystal. The experimentally obtained values of overheating of both crystals are in good agreement with the simulation results (23.8°C and 26.1°C, respectively).

Another way to check the simulation results is based on measuring the thermal radiation from a heated bipolar transistor crystal. The crystal was heated by passing current pulses through the transistor with a duration increasing according to the logarithmic law. The duty cycle of the pulses, set by the operator, is equal to 1. This means that the crystal was heated by direct current with short-term switching from the heating mode to the mode of measuring the TPP – the direct voltage drop on the emitter junction. The duration of the heating process, at the end of which the thermal radiation of the crystal was measured, was estimated based on the analysis of the transient thermal characteristic (TTC), which is the dependence of the thermal impedance on the duration of the heating current pulses. Thermal impedance $Z_T(t)$ was determined according to the expression:

$$Z_T(t) = \frac{T_j(t) - T_j(t=0)}{I_{ht} \cdot U_{ht}}, \quad (7)$$

where $T_j(t)$ – junction temperature at an arbitrary time t; $T_j(t = 0)$ – junction temperature at the initial time; I_{heat} – amplitude of heating current pulses; U_{heat} is the voltage across the transistor. The result of measuring the TSP of transistor No. 2 is presented in **Fig. 7**. From the $Z_T(t)$ graph it is clear that with the duration of heating current pulses in the range from 40 to 800 ms, the value of thermal impedance increases relatively little. This indicates that in this range of pulse durations the crystal is heated, and the substrate temperature changes insignificantly. Therefore, the thermal field from the heated crystals was measured after the duration of the heating pulses reached 800 ms. The pulse amplitude was set to 8.0 A, which ensured a power output of 9.1 W in the transistor.

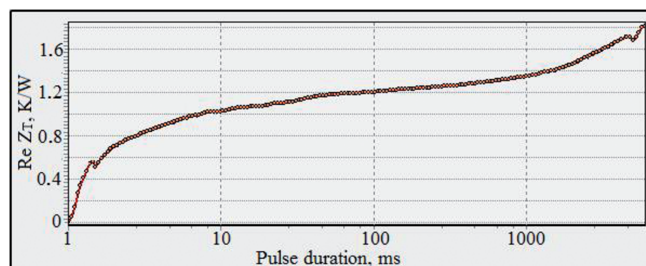

Fig. 7. *Transient thermal response.*

Temperature fields were measured using a Testo 876 thermal imager with an IR thermal imager matrix of 160×120 pixels, a temperature sensitivity of less than 80 mK, and a spectral range from 8 to 14 μm. Since the focal length of the Testo 876 lens is too long for the crystals under study, an additional germanium lens with a focal length of 9 mm was installed [15]. Thermograms of crystals No. 2 and No. 3 of bipolar transistors are presented in **Fig. 8.** For ease of perception of the temperature field, Fig. 8*a* shows an enlarged image of crystal No. 3. A defect in the form of an area of contact between the crystal and the substrate that is not completely filled with adhesive is artificially introduced into the contact connection of this crystal with the substrate.

Using the Testo 876 thermal imager, the temperature of the maximum heated area of the crystal can be determined from the obtained thermograms. For crystal No. 2, the adhesive layer of which does not contain defects, the temperature field of the active region of the crystal is uniform. The temperature of the crystal over the entire surface is approximately the same and is equal to T_2 = 40.5°C. For crystal No. 3 with a defect in the adhesive layer, the temperature distribution over the crystal area is significantly non-uniform. In the defect area, the maximum temperature of the crystal is T_3 = 43.6°C, which is noticeably higher than the average temperature over the crystal. It should be taken into account that accurate determination of the temperature of the crystal surface requires knowledge of the emissivity of silicon, which, in turn, depends on the temperature, surface condition and the presence of an oxide film on the surface of the crystal [16]. Therefore, when comparing the thermal fields of two crystals, only their temperature difference $\Delta T_{32} = T_3 - T_2$ can be correctly assessed. With

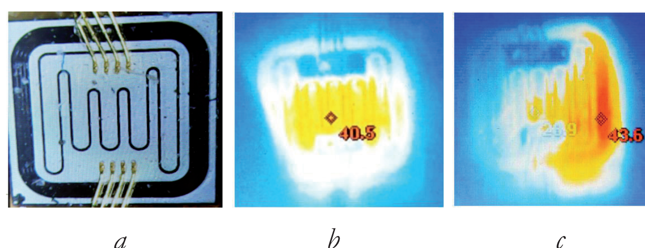

Fig. 8. *Bipolar transistor crystal: a) appearance; b) thermal field of crystal No. 2; c) thermal field of crystal No. 3 (with an adhesive defect).*

the thermal power dissipated in the crystals being 9.1 *W*, the difference is ΔT_{32} = 3.1°C, and when converted to 10 *W* of dissipated power – ΔT_{32} = 3.4°C. The obtained value is approximately 1.5 times higher than the simulation result (ΔT_{32} = 2.3°C). Considering that for crystal No. 3 the thermal field is significantly inhomogeneous, and the average temperature is approximately 1°C lower than the maximum, we can conclude that the results of measuring the difference in average temperatures ΔT_{32} for the two crystals are in fairly good agreement with each other.

6. CONCLUSION

As a result of the research, a thermomechanical model of a multi-crystal system was developed, in which there is a defect in the area of connection through the adhesive of one of the MCS crystals with the substrate. Calculations of temperature and corresponding thermal stresses in various layers of the structure of the modeling object were carried out. Estimates of thermomechanical stresses arising in the adhesive layer due to non-uniform temperature distribution have been made, and the influence of adhesive thickness and defect size on the magnitude of shear stress has been studied. It has been shown that at small values of the adhesive thickness, a sharp increase in the magnitude of the shear stress is observed. For the presented design variant of the structure, reducing the thickness of the adhesive layer by three times leads to an increase in the value of the shear stress to a value that exceeds the limiting value of the shear stress for this type of adhesive by 20%. As the relative defect size K_s increases, the shear stress monotonically increases and reaches a limiting value provided that the defect size is 0.2 of the total contact area of the crystal with the substrate. A comparison of the simulation and experimental results showed that they are in good agreement with each other, which confirms the adequacy of the developed thermomechanical model.

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