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Silicon field nanotransistor with a surrounding gate and a nonlinear geometry of the working area

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Abstract: **A silicon CMOS nanotransistor with a cylindrical geometry with a fully enclosing gate with a non-linear geometry of the working area is discussed. Numerical studies of prototypes with a parabolic working area were performed using mathematical modeling of the instrumental technological simulation performed in the TCAD software environment based on the models of n- and p-type nanotransistors developed by TCAD. An inverter model has been developed for n- and p-type prototypes with an optimized radius ratio of 0.76. At control voltages of 0.6 V and a frequency of 25 GHz, the model predicts a maximum switching delay of 1.0 ps, an active power limit of 0.22 μW, and a static power of 72 pW. The electrophysical characteristics of the n-type prototype with dielectric stacks of gate oxide SiO_2-Al_2O_3 and SiO_2-HfO_2 are analyzed numerically. The simulation results show that the use of high k stacks has a noticeable effect on key transistor characteristics. Thus, a parabolic nanotransistor architecture with an optimized radius ratio can potentially become a replacement for a cylindrical structure for high-speed low-voltage applications.**

Keywords: **silicon nanotransistor architecture, surrounding gate, parabolic profile of the working area, simulation**

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1. INTRODUCTION

Modern design methods and technological processes have unique capabilities for the production of three-dimensional integrated circuit elements. The use of these possibilities has made the gate-all-around (GAA) transistor family a priority for the modern technological development of nanoelectronics [1,2]. However, the negative properties of such transistors are a large subthreshold current and a high steepness

of the subthreshold characteristic [2,4-6]. This is the result of scaling up to increase the speed of nanotransistor VLSI. In this paper, based on the approach associated with changing the geometry of the transistor's working area [7–9] to overcome the effects of scaling, a new member of the GAA family was developed and its electrophysical characteristics were investigated.

In this paper, a cylindrical CMOS architecture of a nanotransistor with a surrounding gate and a working area in the form of a truncated paraboloid is developed, where the radius of the working area from the drain side is less than its radius from the source side. In this configuration, partial screening of the drain is implemented. This reduces the influence of hot carriers, which leads to an increase in the drain current of the transistor [10,11]. And also complicates the diffusion of carriers in the subthreshold mode. In such an architecture, it becomes possible to more effectively suppress short-channel effects (SEC), reduce capacity, which causes prerequisites for increasing performance and reducing the level of power dissipation [11-14].

The potential application possibilities of silicon cylindrical prototypes with a surrounding gate of sub 25 nm CMOS transistors with a working area in the form of a truncated paraboloid for low-voltage digital applications are numerically investigated [3,11,15,16]. The research is carried out using TCAD instrument-technological modeling [17]. Based on the TCAD model of a silicon cylindrical CMOS nanotransistor with a working area in the form of a truncated paraboloid developed within the framework of this work, the electrophysical characteristics of *n*- and *p*-type transistor structures with a low level of control voltages are analyzed. Estimates of their operability have been obtained. Based on these models, a high-frequency low-voltage inverter has been synthesized. The influence of dielectrics with high dielectric permittivity on the electro-physical characteristics of the transistor structure under consideration has been studied.

2. TRANSISTOR PROTOTYPE STRUCTURE

Fig. 1 shows a 3D sketch of the architecture of a silicon cylindrical CMOS nanotransistor with a working area in the form of a truncated paraboloid. It includes the source (pos. 1), the drain (pos. 2), and the working area (slot. 3), where L_g is the length of the working area along the symmetry axis along the *z* axis. The

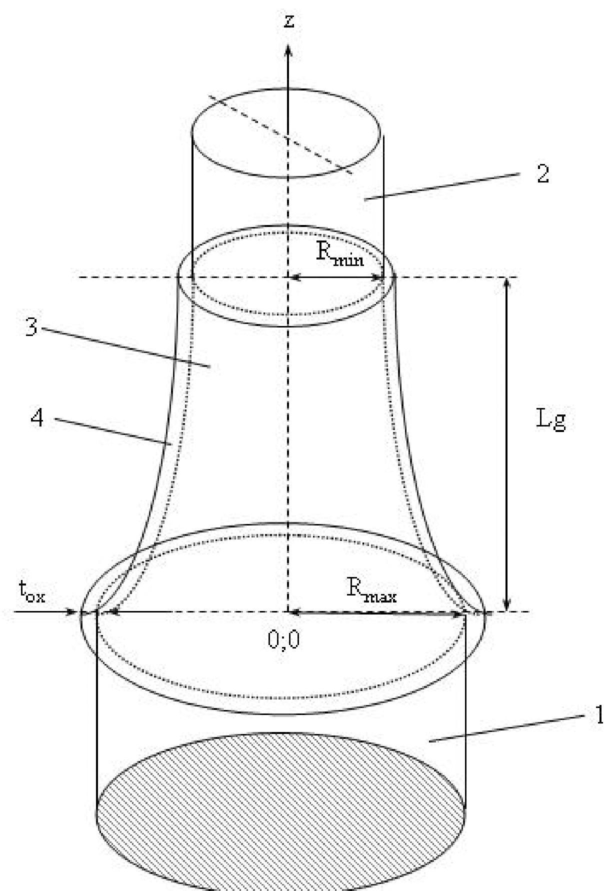

Fig. 1. *Block diagram of a silicon cylindrical CMOS nanotransistor with a surrounding gate with a parabolic working area, where 1 is the source, 2 is the drain, 3 is the working area, 4 is the gate dielectric with a thickness of t_{ox}, L_g is the length of the working area, R_{max} is the radius of the working area from the source, R_{min} is the radius of the working area from the drain side.*

silicon core of the working area is completely covered by a silicon oxide film (pos. 4) with a thickness of t_{ox} and a polysilicon gate with a thickness of t_g (not shown in the figure).

When choosing geometric parameters, the following should be taken into account. When scaling cylindrical transistor structures, only a decrease in the radius of the working area (R) leads to a decrease in the transistor current [12]. In order to suppress SCE in a cylindrical architecture, a condition binding geometric parameters must be fulfilled: $L_g \le 12.2\sqrt{Rt_{ox}}$ [12,18]. The fulfillment of this condition determined the design of a cylindrical nanotransistor with a surrounding gate CMOS with a working area in the form of a truncated paraboloid. In this case, from the source side for a larger radius (or R_{max}), the condition of SCE suppression is not fulfilled, and from the drain side for a small radius (R_{min}), it is fulfilled. In this case, the dependence of the radius change can be written as follows:

$R(z) = R_{\min} + \frac{\Delta R}{L_g^2}(L_g - z)^2$ and $\Delta R << L_g$,
where $\Delta R = R_{max} - R_{min}$.

The problem of calculating the electrophysical characteristics of the analyzed transistor structure is solved for the minimum possible L_g, R_{max}, R_{min} and t_{ox} from the range of values close to the miniaturization boundary [1,14-16].

To minimize the capacitive coupling of the gate-source and gate-drain, the transition between them is made in the form of a truncated cone [9] (see **Fig. 2**).

In this case, the gap between the gate and the source (drain) will increase linearly along the *z*-axis. The ratio L_{g_ds}/l_{g_ds}, where L_{g_ds} and l_{g_ds} are the maximum and minimum distance between the gate and the drain (source), is a boundary condition for the level of capacitive coupling [13,14].

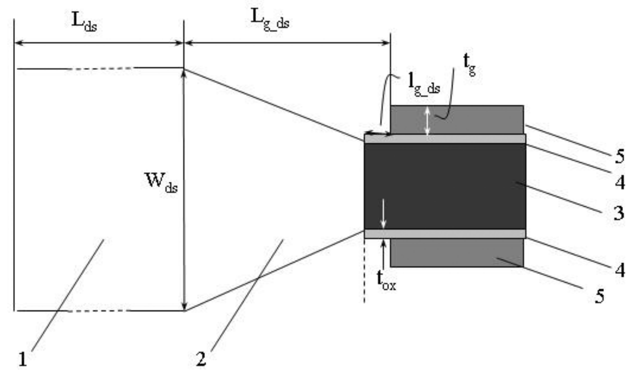

Fig. 2. *Block diagram of the drain (source)-gate node, where 1 is the drain (source), 2 is the conical junction, 3 is the silicon core of the working area, 4 is the gate dielectric, 5 is the polysilicon gate, L_{ds}, W_{ds} are the longitudinal and transverse dimensions drain (source), respectively, L_{g_ds}, l_{g_ds} is the maximum and minimum distance between the gate and the drain (source), respectively, t_{ox} is the thickness of the gate dielectric, t_g is the thickness of the gate.*

3. PROTOTYPE MODEL AND SIMULATION SETUP

When choosing the topological parameters of transistor prototypes, it is necessary to take into account that when scaling, a decrease in the total number of carriers involved in the transfer process will have a critical impact. The direct increase in the diameter of the active region is limited due to the fact that the efficiency of suppression of SCE is reduced [19]. The increase in the doping level of the source and drain is also limited by an exponential increase in the direct tunnel current between them and a decrease in the breakdown voltage [10,20].

A TCAD model has been developed for a silicon cylindrical surrounding gate CMOS nanotransistor with a working area in the form of a truncated paraboloid. The "vertical" was considered (see Fig. 1) a variant of the transistor design taking into account the surface recombination of charge carriers by the Shockley-Reed-Hall mechanism, high degradation of field mobility [21]. In our calculations, the radii ratio R_{min}/R_{max} varied in the range of 0.6-1, where the maximum value of R_{min}/R_{max} corresponds to the generally

accepted cylindrical configuration of the GAA transistor. The value of the L_g parameter is fixed. The effect of the floating base is compensated by the choice of the range of variation of the radius of the silicon core of the working area [19]. The thickness of t_{ox} is set so as to exclude the influence of the constant tunnel current of the gate. Based on the technological requirements for the thickness t_g and the transverse size of the high-alloyed drain/source W_{ds}, the value of the parameter L_{g_ds} is minimized. It is found from the following conditions: 1)$L_{g_ds} > (t_g + t_{ox})$; 2) $L_{g_ds}/l_{g_ds} > 15$; 3) $l_{g_ds} > 1.0$ nm, the performance of which provides a very weak capacitive load [13,14], which is a good compensation for the parasitic capacitances of this node, affecting the electrophysical characteristics of the transistor. In the simulation, the lattice temperature is fixed.

In the course of numerical experiments, prototypes with different R_{min}/R_{max} ratios were analyzed. The main model parameters of the prototypes are shown in **Table 1**.

In Table 1 the designations not defined above have the following meanings. L_{ds}, N_{ds} are the longitudinal size and doping concentration of the source and drain, respectively; v_{SRH} and t_{SRH} are the surface recombination rate and the lifetime of non-basic charge carriers by the Shockley-Reed-Hall mechanism, respectively.

To model the analyzed transistor architecture, the structural design module SDE of the ISE TCAD package was used [17]. At the same time, the geometric boundaries of the regions were set strictly, without modeling technological processes. The calculation of the electrophysical parameters of the prototypes is carried out by numerical methods on grid nodes with an optimized step. In the drain and source areas with a constant radius, the grid pitch is increased. In regions with a variable radius, where the main physical processes of charge carrier transfer take place, the grid pitch decreases. The exact dimensions of the minimum and maximum grid steps, as well as the law of transition between them, are selected empirically. The SNMesh software module was used as an optimizer of the computational grid. The basis for numerical modeling of the electrophysical parameters of prototypes is the solution of a system of partial differential equations describing the static and dynamic behavior of carriers in a nanotransistor structure under the action of control voltages at the gate and drain [22]. This system of equations is solved using the SDevice software module by the grid method using the Newton algorithm under variable boundary conditions, as well as taking into account the corresponding models of physical processes occurring in active regions.

Table 1

Main parameters of prototypes

Parameter	Value	Parameter	Value
L_g, nm	22	N_A,cm^{-3}	1.5x1015
R_{max}, nm	5	L_{ds}, nm	50
R_{min}, nm	3-5	W_{ds}, nm	50
t_{ox}, nm	1.5	N_{ds},cm^{-3}	5x1019
t_g, nm	15	v_{SRH}, cm/sec	3x105
L_{s_ds}, nm	22	t_{SRH}, μs	10
l_{g_ds}, nm	1.0	T, K	300

4. SIMULATION RESULTS AND DISCUSSION

Modeling of electrophysical characteristics of prototypes of a silicon CMOS nanotransistor with a cylindrical geometry, a surrounding gate and a parabolic working area was carried out in the range of control voltages from 0 to 0.6 V.

Fig. 3 shows the values of the maximum current of *n*-type prototypes, extracted from the results of calculations of I-V data characteristics at different values of R_{min}/R_{max} in the range of 0.6-1. It should be noted that

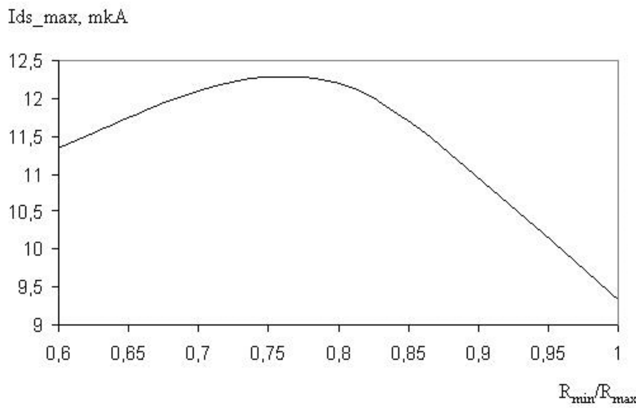

Fig. 3. *Dependence of the maximum current of prototypes (I_{ds_max}) at $U_{ds} = U_{gs} = 0.6$ V on R_{min}/R_{max}.*

the analyzed prototypes function in the normal mode in accordance with classical concepts [2]. In all cases, the drain current of the *n*-type prototype is approximately 2 times higher than the drain current of the *p*-type prototype.

It can be seen from Fig. 3 that a parabolic structure in a large range of R_{min}/R_{max} is characterized by a large drain current compared to the cylindrical one. The increase in the drain current is associated with a more uniform distribution of carriers in the cross section of the working area, which occurs due to its narrowing at the drain. In this case, the most favorable conditions are created for the transport of carriers. First, the minimum number of hot media. Secondly, the high accelerating potential. The combination of these factors determines the most effective transfer of media to the drain [3,5,7]. In experiments, the maximum current is 12.3 μA at R_{min}/R_{max} = 0.76. Compared to a cylindrical working area (R_{min}/R_{max} = 1), the maximum drain current is approximately 3 μA higher, or 24%. With a decrease in the value of R_{min}/R_{max}, the silicon thickness at the drain decreases, which negatively affects the mobility of carriers and, consequently, the conductivity of the device. At large values of R_{min}/R_{max} (> 0.8), the drain current decreases due to a decrease in the efficiency of drain shielding. It should be noted that from the simulation results it follows that the maximum conductivity also corresponds to the ratio R_{min}/R_{max} = 0.76, obviously due to the best conditions for carrier transport. Therefore, the optimized prototype will have the highest gain.

For low-voltage high-speed applications, the study of the following parameters: I_{off} current, subthreshold slope (SS), I_{on}/I_{off} current ratio. They are of fundamental importance for assessing the applicability of a particular transistor structure in high-performance digital circuits. So the I_{off} current reduces the turn-on current, which affects the performance of the transistor and the chip as a whole, and determines the level of the energy budget and noise immunity of the circuit [3,15,16]. The SS parameter is important to ensure the required static and dynamic characteristics of nanotransistors. In **Fig. 4** for the *n*-type prototype, the extracted values of the I_{off} and SS parameters are given.

From Fig. 4, where the simulation results are presented, it can be concluded that parabolic prototypes provide a lower leakage current compared to the cylindrical design. For an optimized transistor structure, R_{min}/R_{max} = 0.76, SS = 66.8 mV/dec. With an increase in the R_{min}/R_{max} ratio, a steady increase in SS is observed, which indicates an increase in the

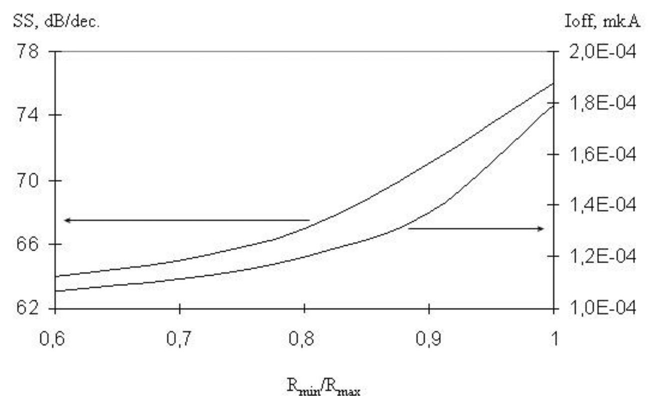

Fig. 4. *Dependence of I_{off} current and the SS subthreshold slope on R_{min}/R_{max} at U_{ds} = 0.6 V.*

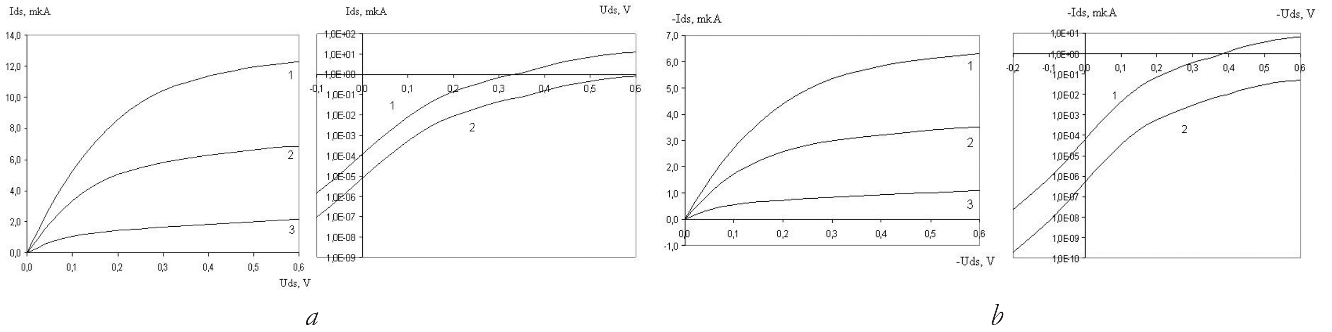

Fig. 5. *I-V data prototypes with optimized R_{min}/R_{max} ratio, where a) n-type prototype, left figure $I_{ds}(U_{ds})$ at 1– U_{gs} = 0.6 V, 2–U_{gs} = 0.4 V, U_{gs} = 0.2 V, right figure $I_{ds}(U_{gs})$ 1 – U_{ds} = 0.05 V, 2 – U_{ds} = 0.6 V; b) p-type prototype, left figure $I_{ds}(U_{ds})$ at 1–U_{gs} = –0.6 V, 2 – U_{gs} = –0.4 V, U_{gs} = –0.2 V, right figure $I_{ds}(U_{gs})$ 1–U_{ds} = –0.05 V, 2 – U_{ds} = –0.6 V*

influence of the SCE and limits the range of possible values of the R_{min}/R_{max} parameter. When developing modern electronic devices, it is important to take into account the ratio of I_{on}/I_{off} currents [15]. For an optimized transistor structure, this current ratio is 5 orders of magnitude.

Fig. 5 shows the I-V data $I_{ds}(U_{ds})$ and $I_{ds}(U_{gs})$ for *n*- and *p*-type transistor structures with an optimized ratio of radii.

The totality of the data obtained allows us to assert that the transistor structure in question can potentially be used for high-speed digital applications.

5. INVERTER SYNTHESIS

With the help of the TCAD program, using the models of the studied transistor structures of *n*- and *p*-types of conductivity developed in this paper, the propagation of a high-frequency logic signal through an inverter on prototypes with optimized topology is simulated. A sketch of the placement of transistors included in the inverter is presented in [22].

For this inverter, the transfer characteristic is modeled for various values of the U_{dd} supply voltage in the range from 0.3 to 0.6 V. The family of transfer characteristics $U_{out}(U_{in})$ is shown in **Fig. 6**, where the voltage U_{in} corresponds to U_{gs}.

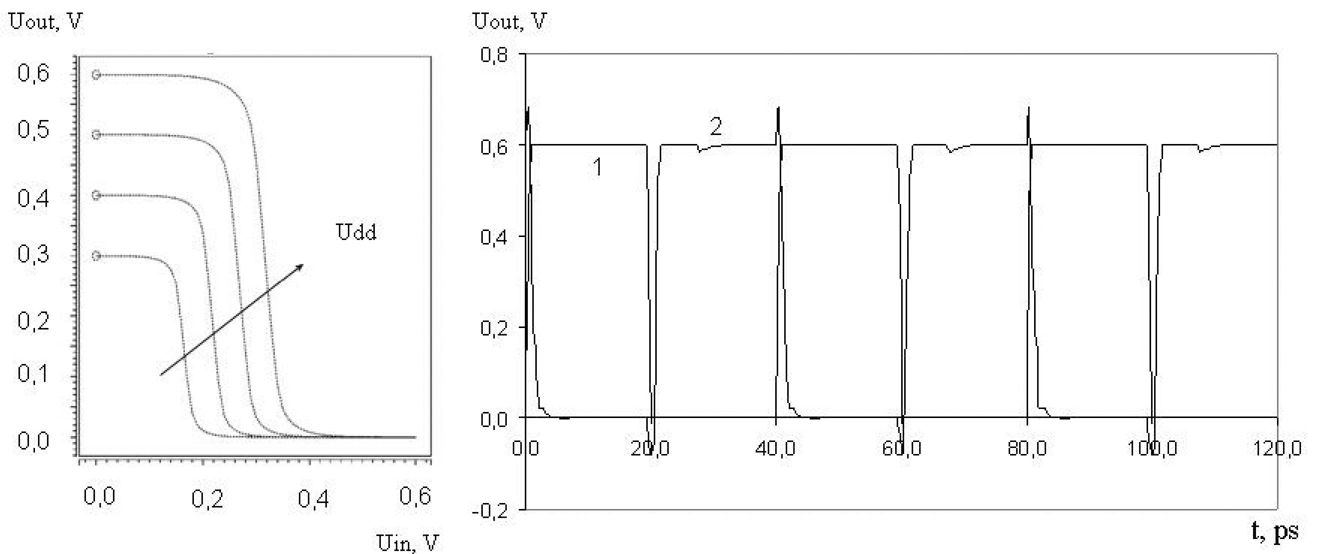

Fig. 6. *Characteristics of the inverter, where the left figure is a family of transfer characteristics when U_{dd} changes from 0.3 to 0.6 V, the right figure is the dynamic characteristic of the inverter at U_{dd} = 0.6 V, where 1 is the clock (input) signal, 2 is the response of the inverter.*

Table 2

Inverter specifications

Parameters		
τ_{in}/τ_{out}, ps	P, μW	$P_{стат}$, pW
1.0/0.45	0.22	72

The simulation results show that the operability of all devices is maintained in a wide range of U_{dd}. What is noteworthy is that in the region of low applied voltages (less than 0.6 V), they function close to an ideal inverter with a high voltage gain [3,16].

The dynamic characteristics of each prototype in the large high frequency signal mode were calculated for an unloaded device for an input signal with an amplitude of 0.6 V and a clock frequency of 25 GHz. The results of inverter switching simulation at U_{dd} = 0.6 V are shown in Fig. 6. It should be noted that the valve transmits the pulse sequence practically without distortion. The extracted values of delay and power (active and static) are given in **Table 2**.

The data obtained confirm that the transistor structure under consideration can potentially be used for high-speed digital applications.

6. APPLICATION OF DIELECTRICS WITH HIGH k

Dielectric materials of the silicon field-effect transistor gate have played a significant role in the development of modern nanoscale electronic devices with high performance characteristics [19,23-24]. In this case, *high-k* dielectrics are considered in conjunction with an interface layer, the role of which is played by a silicon oxide film SiO_2. This design is called a dielectric stack. Interface layers are created intentionally in order to passivate the surface, prevent diffusion, or increase adhesion. This is due to the better quality of the Si-SiO_2 interface, which is formed during the manufacturing process. Materials with *high-k* are more suitable than traditional silicon oxide SiO_2, due to the lower required film thickness of the gate dielectric. This leads to a decrease in the threshold voltage and an improvement in the subthreshold characteristics of the field-effect transistor [16,19,24]. Therefore, it is an urgent task to investigate the change in the electrophysical characteristics of a transistor with the transition to a stack gate dielectric.

Fig. 7 shows the cross section of the workspace. Its silicon core (pos. 1) is completely covered by a 0.5 nm thick silicon oxide film (pos. 2), and on top of it is surrounded by a 1 nm thick dielectric film with a *high-k* (pos. 3).

The TCAD model presented above has been extended to simulate transistor electrophysical characteristics, taking into account the stack design of the gate dielectric. It should be noted that interface layers can somewhat reduce the capacitance of the *high-k* dielectric layer [25]. Regardless of which interface layer was formed, the total electrical capacitance of the stack will be less than the capacity of the *high-k* film itself.

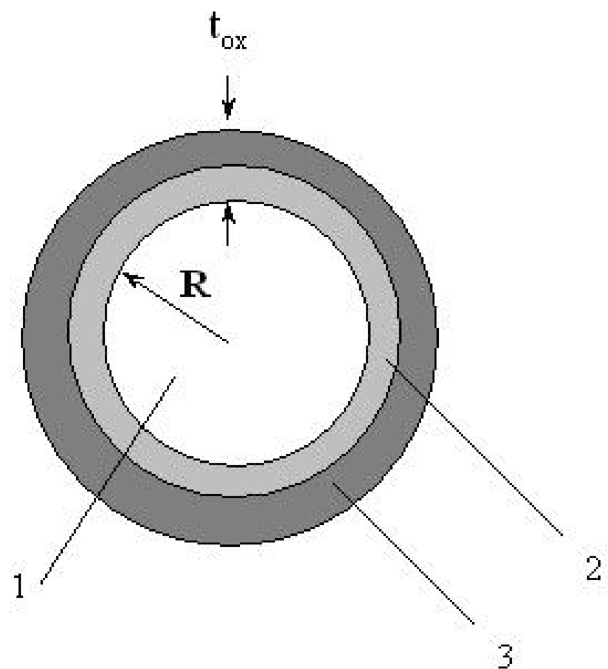

Fig. 7. *Sketch of the orthogonal section of the working area, where 1 is the silicon core of the working area, 2 is a silicon oxide film, and 3 is a dielectric film with high k.*

Table 3

Main parameters of prototypes

stek	I_{ds_max}, μA	*SS*, mV/dec	I_{off}, μA	I_{on}/I_{off}
SiO_2-Al_2O_3	13.9	64.5	3,5x10-05	4.0x10+05
SiO_2-HfO_2	15.2	63.6	1,2x10-05	1.3x10+06

For an *n*-type prototype with an optimized transistor structure with two different stacks (hafnium dioxide HfO_2 (k = 25) and aluminum oxide Al_2O_3 (k = 9.3) – the top film of the stack), **Table 3** shows the values of I_{ds_ma}, I_{off}, *SS* and I_{on}/I_{off}, extracted from the simulation results.

According to these data obtained above, as the stack dielectric constant increases, the drain current increases, and the subthreshold slope decreases. Therefore, a silicon field-effect transistor with a fully enveloping gate with SiO_2-HfO_2 glass seems to be the most interesting for digital applications [3,15,16]. This property is due to the highest electrostatic controllability of the working area by the gate, which completely controls all media located in the working area and ensures their accentuated transfer from source to drain.

However, the physical and chemical nature of the origin of degradation mechanisms in dielectric glass remains unclear. Among all the defects of the crystal lattice, the most important role is most likely played by interstitial oxygen atoms and positively charged oxygen vacancies, which can potentially have a different (in the limit – differently polar) effect on the carrier transfer process in the working area [26-28].

5. CONCLUSION

The design of a silicon cylindrical CMOS nanotransistor with a surrounding gate and a longitudinal parabolic profile of the working area has been developed and investigated. To compensate for the SCE from the source side for a large diameter of the working area, the SCE suppression condition is not met, and from the drain side for a small diameter, it is fulfilled. TCAD models of *n*- and *p*-type transistor prototypes with a working area length of 22 nm, with a fixed large radius of 5 nm and a variable small radius of 3 nm have been developed. In the range of control voltages 0...0.6 V, the behavior of the drain current, subthreshold slope and leakage current is numerically investigated depending on the value of the ratio of radii. It follows from the results obtained that the parabolic geometry with a radius ratio of 0.76 provides the highest drain current of 12.3 mA, demonstrates the maximum I_{on}/I_{off} ratio of ~10^5 and the steepness value of the subthreshold characteristic of 66.8 dB/des.

Based on the prototypes of *n*- and *p*-types, a basic logic element, an inverter, has been synthesized. Its static and dynamic characteristics are numerically investigated. At control voltages of 0.6 V and a frequency of 25 GHz, the inverter model predicts a maximum switching delay of 1.0 ps, an active power limit of 0.22 μW, and a static power of 72 pW.

The electrophysical characteristics of an *n*-type prototype with SiO_2-Al_2O_3 and SiO_2-HfO_2 dielectric stacks are numerically analyzed. The results of numerical simulation show that the use of stacks with *high k* has a noticeable effect on the key characteristics of the transistor compared to silicon oxide. This is due to the fact that the effect of the gate on the characteristics of the transistor structure, especially in the subthreshold region, decreases, which can be partially compensated by the use of dielectrics with *high k*.

The results obtained allow us to attribute the transistor structure with a parabolic geometry of the working area to highly competitive in the gate-all-around transistor family.

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