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Simulation of the characteristics of low-voltage gates on combined cylindrical surrounding gate field-effect nanotransistors

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Abstract: **The applicability of the architecture of a nanoscale surrounding gate field-effect transistor with a combined cylindrical working area for low-voltage applications is discussed. At the same time, the licensed TCAD Sentaurus instrument and technological modeling system is used as a tool. The transistor architecture under consideration involves combining the working zones of n-channel and p-channel transistors with one common gate. At the same time, the efficiency of suppressing short-channel effects is maintained and a high level of transistor current is provided in the strong inversion mode. Based on this architecture, a TCAD model of the NAND gate has been developed, the design of which contains two independent surrounding gates one combined working area. The use of the proposed gate architecture makes it possible to reduce the number of required transistor structures per gate by three times. This leads to a decrease in the switched capacity and power dissipation. From the simulation results, the gate geometric parameters with a working area length of 25 nm and a diameter of 8.5 nm, which can function at control voltages of 0.5 V in the frequency range up to 20 GHz with high gain, are determined. The switching time delay is 0.81 ps. The TCAD model of a half-adder is developed in the basis 2NAND. According to the simulation results, the efficiency of the prototype, which performs binary code addition operations with a delay of 4.2 ps at a supply voltage of 0.5 V and a frequency of 20 GHz, is shown. The obtained results create a theoretical basis for the synthesis of low-voltage complex functional blocks with high performance and minimal occupied area, which meets modern requirements for digital applications.**

Keywords: **nanoscale MOSFET, silicon on insulator, surrounding gate, short-channel effects, logic gate, low supply voltage**

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Contents

1. INTRODUCTION

The main direction of development of modern microelectronics – "More Moore and more than Moore" also covers the creation of nanotransistor architectures that can provide ultra-high performance and an exorbitant degree of integration [1]. Among them, those in which the active zone (channel) is completely surrounded by a gate predominate [1-5]. One of these is the architecture with cylindrical geometry [6]. It is characterized by a twofold superiority in suppressing short-channel effects (SCE) in comparison with traditional transistor architectures. It also features improved subthreshold performance and increased current density in strong inversion mode [6-9]. A creative development of a cylindrical architecture with a fully surrounding gate is the concept of combining *n*- and *p*-type transistors into a single whole [10], that is shown on **Fig. 1**.

In this case, the source and drain regions are divided into two highly alloyed *n*- and *p*-types, the working region is universal for charge carriers (electrons and holes). The entire transistor structure is placed on a SOI (silicon on insulator) substrate. A distinctive feature of such a design is the ability to significantly increase the degree of integration [11,12], and also allows for a wide variety of design designs [1,2,10-14], which will greatly simplify the task of designing complex-functional logic gates [2,10]. To achieve high conductivity of the considered transistor structure, it is necessary that its working region be low-alloyed. Ideally, its conductivity will be close to the intrinsic conductivity of silicon [7,15,16]. When the supply voltage (U_{dd}) is applied to the source, the process of carrier injection into the combined working region is activated [10,17]. Their distribution in the channel depends on the gate voltage (U_g). Thus, at $U_g - U_{th} > 0$, electrons prevail in the channel, and at $U_g - U_{th} < 0$ – these are holes, where U_{th} is the threshold voltage. Therefore, the considered transistor structure is a single-stage logic gate, whose input is the gate, the output is a common drain [6,9].

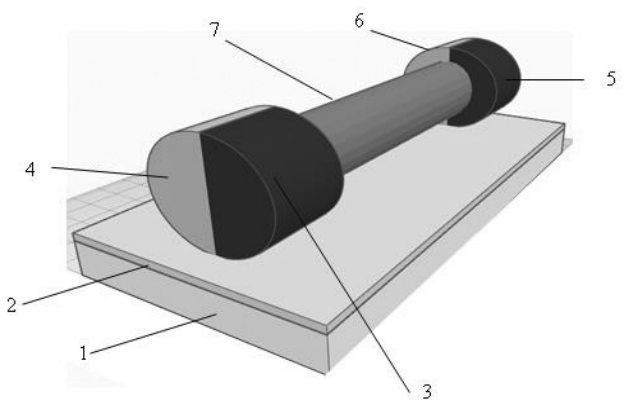

Fig. 1. *Block diagram of the combined transistor. Here 1 is the silicon substrate, 2 is the silicon oxide, 3 is the n^+-source, 4 is the p^+-source, 5 is the n^+-drain, 6 is the p^+-drain, 7 is the combined working region.*

On the basis of the developed transistor, it is possible to synthesize a more complex logic gate NAND. **Fig. 2** shows a functional diagram of a two-input NAND gate based on one transistor with two independent fully surrounding gates.

The current flows through the gate only if the voltage corresponding to the level of the logical unit U_1 ($U_1 = U_{dd}$) is applied to both gates at the same time. Then the voltage at the output (drain) will be low, close to zero, equal to the logic zero level U_0. For all other combinations of gate voltages, in the ideal case, no current will flow through the gate,

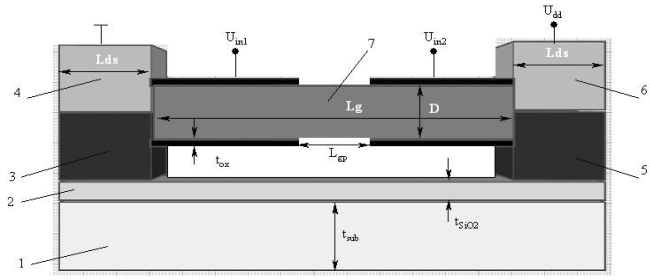

Fig. 2. *Block diagram of the 2NAND gate, where where the numerical designations correspond to Fig. 1. Here, L_g is the length of the working area, D is the diameter of the working area, L_{ds} is the size of the source and drain regions, t_{ox} is the thickness of the gate dielectric, L_{gp} is the size of the gap between of independent gates, t_{SiO2} is the isolating silicon oxide thickness, t_{sub} is the silicon substrate thickness, U_{dd} is supply voltage, $U_{in1(2)}$ is control voltage.*

and the output voltage will be high, at a logic-one level.

The structure we study is characterized by effective suppression of SCE and low capacitance value. This, together with a reduction in the footprint, leads to a decrease in the level of dissipated power [2,6,7,9], which fully meets the requirements for modern digital circuits [1,4,18].

In this paper, we investigate the possibility of synthesizing complex logic gates combined in nanotransistors with a fully enclosing gate for low-voltage digital applications. The solution of this problem is carried out using the software package of instrument-technological modeling TCAD [19].

2. SIMULATION RESULT OF THE 2NAND GATE

Computer simulation of the electro-physical characteristics of transistor structures was carried out using the DESSIS program of the ISE TCAD package [19]. A TCAD model has been developed for a combined SOI CMOS nanotransistor with a cylindrical geometry and a fully surrounding gate. In the course of numerical experiments, devices with different geometric dimensions of the working region were analyzed, the main parameters of which are given in **Table 1**. The "planar" and "vertical" versions of the gate design were considered, taking into account the surface recombination of charge carriers according to the Shockley-Reed-Hall mechanism, high degradation of the field mobility, and without taking into account quantum effects. The following designations are adopted in Table 1. Here t_{ox} is the gate oxide thickness (silicon oxide), t_{SiO2} is the silicon oxide thickness, t_{sub} is the silicon substrate thickness, n_i is the intrinsic carrier concentration, L_{ds} is the drain and source length, N_{ds} is the source and drain alloying concentration, v_{SRH} is the surface recombination rate by the mechanism Shockley-Reed-Hall, t_{SRH} is the lifetime of minority charge carriers according to the Shockley-Reed-Hall mechanism, A_d is the output function.

In our calculations the diameter D, the gate length L_g, and the length of the gap between the gate oxide of independent gates L_{gp} are varied. When choosing the parameters L_g and D, it is necessary to fulfill the condition of complete suppression of the SCE [6]. It should be borne in mind that with a decrease in the diameter, the

Table 1

The main parameters of prototypes

Parameter	Value	Parameter	Value
Lg, nm	22...32	*D*, nm	8...12
Lgp, nm	5...8	t_{ox}, nm	1.2
t_{sio2}, nm	20	t_{sub}, μm	0.6
Lds, nm	100	n_i, cm^{-3}	10^{13}
N_{ds}, cm^{-3}	$3.5 \cdot 10^{19}$	v_{SRH}, cm/s	$3 \cdot 10^5$
t_{SRH},μs	10	A_d, eV	4.65

capacitance of the drain-source junction decreases, and accordingly the threshold voltage increases, and, consequently, the response time of the transistor [16,17,20]. When choosing the topological parameters of the prototypes of the gate, it is necessary to take into account that during scaling, a decrease in the total number of carriers participating in the transfer process will be critical. The direct increase in the diameter of the active region is limited due to the fact that the efficiency of suppression of the SCE decreases [7]. An increase in the alloy level of the source and drain is limited by an exponential increase in the forward tunneling current between the source and drain [4,17,21] and a decrease in the breakdown voltage [20].

At the simulation it is assumed that the boundaries of the working region and the source/drain are sharp. There is no overlap between the gate and the source and drain regions. The t_{ox} thickness is chosen in such a way as to exclude the influence of the constant tunneling current of the gate [7].

From the simulation results, we selected a prototype with the following set a parameters for further research: L_g is equal 25 nm, D is equal 8.5 nm, L_{gp} is equal 6 nm, since ratio of the its ON/OFF currents was maximum, more than 10^6, which is the main criterion for choosing structures for digital applications [10, 22].

Fig. 3 shows the TCAD simulation result of the distribution of carriers in the working region of the chosen gate for the control gate voltages $U_{in1} = U_{in2} = U_0$ and the supply voltage $U_{dd} = 0.5$ V. In this case, the working region is mainly filled with holes and its electronic conductivity is very low.

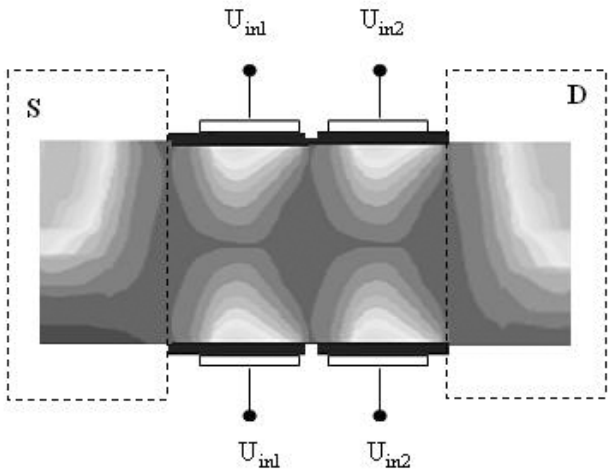

Fig. 3. *Fragment of the distribution of carriers in its active region of the NAND gate.*

Fig. 4 shows the simulation results of the transfer and transient characteristics of the chosen gate. The transfer characteristics of the gate show that it can operate in the

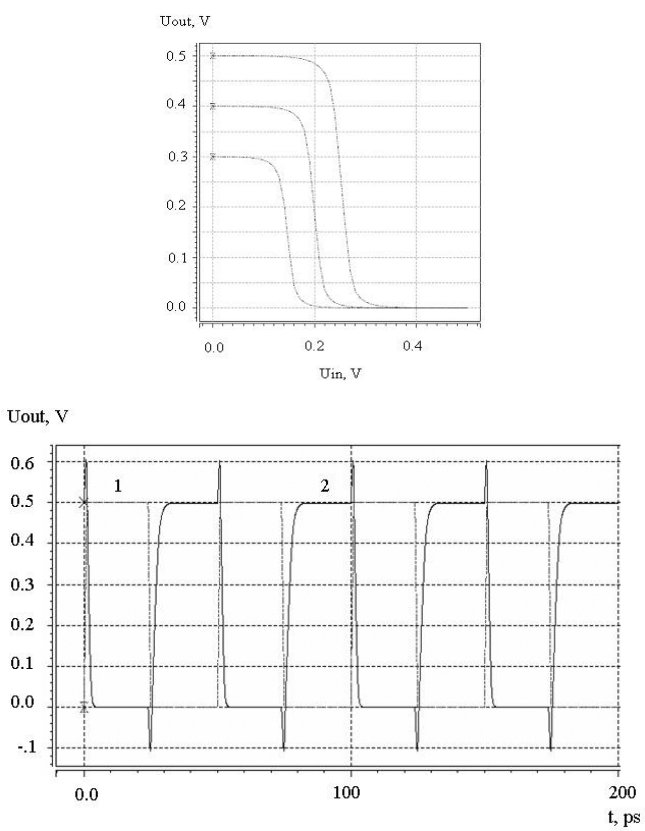

Fig. 4. *(top) A family of transfer characteristics of the gate at U_{dd} from 0.5 to 0.3 V; (bottom) The transient response of the gate at $U_{in2} = U_{dd} = 0.5$ V, where 1 is the input signal U_{in1}, 2 is the output signal (solid line).*

region of low supply voltages (less than 0.5 V) with a high voltage gain. In the given case of the transient response, the gate is triggered and a logical unit signal is generated at its output. The switching time delay at 20 GHz is 0.81 ps. In all other combinations of gate voltages, the voltage at the output of the device corresponds to the logic zero level. In the general case, the response time of the gate is limited by the time response of the transistor structure, which can be optimized by selecting the topological parameters.

3. SIMULATION OF THE CHARACTERISTICS OF A HALF ADDER

The logic element half adder is the main component of a one-digit full adder. It has two inputs a_1 and a_2 for two terms and two outputs: S – sum, P – carry. It is not single-stage due to its logical function. **Fig. 5** shows the implementation of a half adder in the NAND basis. It should be noted that one of the gates in the circuit is used as an inverter, and there are five inverting operations in total. The use of the considered gate architecture leads to a sharp reduction of footprint (at least five times), which increases the fast performance by switched capacitance, and causes a decrease in the dissipated power.

On the basis of the model of the NAND gate, a TCAD model of the half adder was developed. On **Fig. 6** is shown the simulation results one of its possible dynamic characteristics.

Here, at U_{dd} = 0.5 V, the voltage at the input a_1 (U_{a1}) is at a low level "U_0" (0 V) and the voltage at the input a_2 (U_{a2}) is switched from U_0 (zero) to U_1 (one), the output S (US) is switched to the high level of U_1, and the output P (UP) remains at the low level U_0. In the case under consideration, this process occurs with a clock frequency of 20 GHz. Switching time delay is 4.2 ps, switching power is 0.66 μW, static power is 21.5 pW. Depending on the voltage level at the gate inputs, the outputs are maintained either low/low, high/low, or low/high. The presence of peaks is associated with transients in the circuit, the maximum peak value directly depends on the value of the supply voltage.

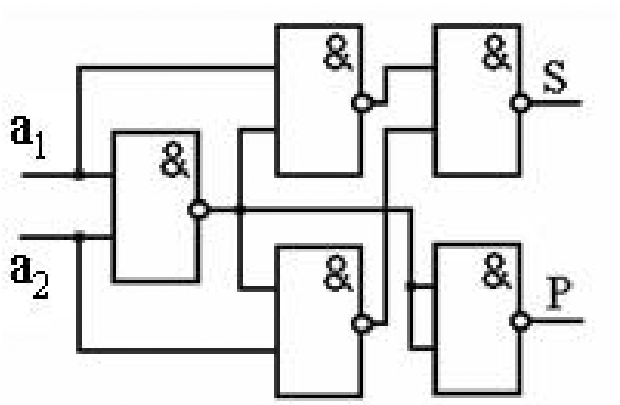

Fig. 5. *Structural circuit of half adder.*

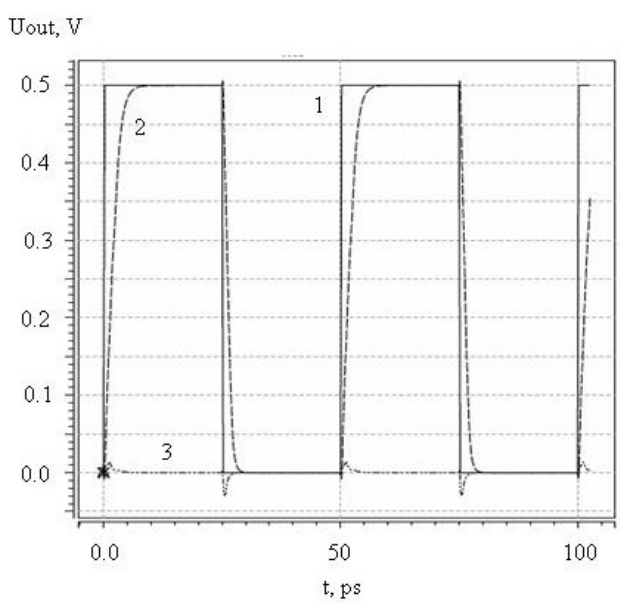

Fig. 6. *Dynamic characteristic of a half adder at $U_{a1} = U_{dd} = 0.5$ V and a clock frequency of 20 GHz, where 1 – U_{a2}, 2 – U_S, 3 – U_P.*

Fig. 7 shows a timing diagram of the voltages at the inputs and outputs of the half adder. The duration of the pulses supplied to each input a_1 (U_{a1}) and a_2 (U_{a2}) is the same. The frequency of their repetition is exactly two times different. This entails the superposition of pulses from the low-frequency sequence U_{a1} on the even pulses of the high-frequency sequence U_{a2}. It is in these cases that the transition of the output P occurs and a signal of a logical unit is formed on it, and a signal of a logical zero is formed at the output S.

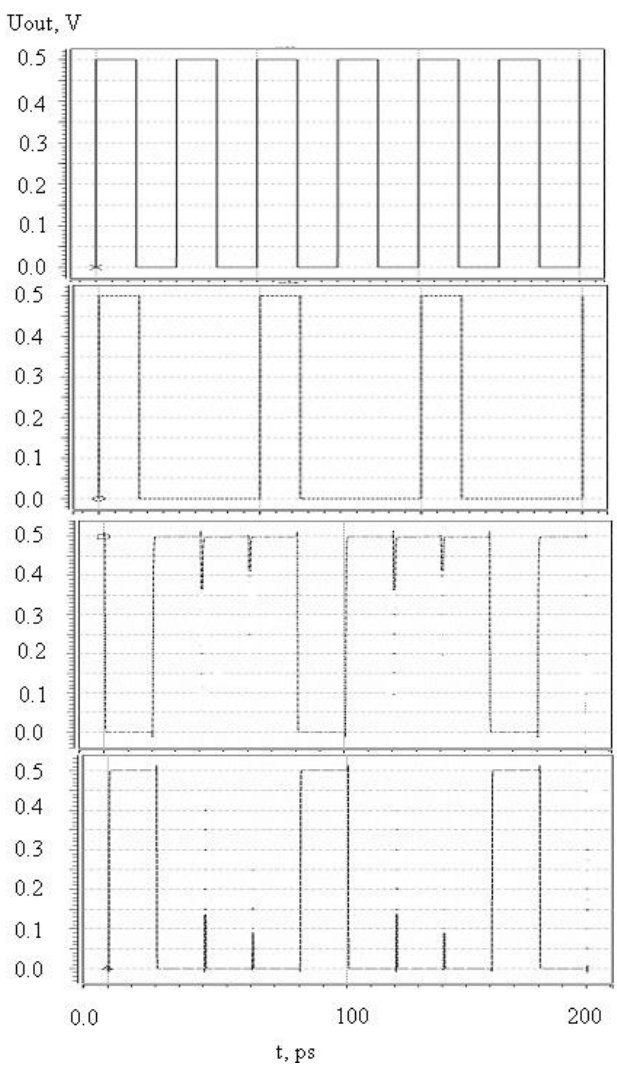

Fig. 7. *Timing diagram of voltages at the inputs and outputs of the half adder, where the two upper figures are the voltage at the inputs a_1 and a_2, the middle one is at the output S, the lower one is at the output P.*

In all other cases, the voltage at the S output corresponds to the level of a logical unit, at the P output – to a logical zero.

Summarizing the results obtained, it can be assumed that devices based on the considered gate architecture can be used in the development of analog and digital circuits applicable for both high-frequency and low-voltage applications.

4. CONCLUSION

The high potential for applicability in low-voltage digital applications of the surrounding gate field-effect nanotransistor architecture with a cylindrical combined working area is shown. At the same time, the licensed instrument and technological modeling system TCAD is used as a tool. Based on this architecture, a TCAD model of the NAND gate has been developed, the design of which contains two independent surrounding gates one combined working area. The use of the proposed gate architecture makes it possible to reduce the number of required transistor structures per gate by three times. From the simulation results, the gate geometric parameters with a working area length of 25 nm and a diameter of 8.5 nm, which can function at control voltages of 0.5 V and lower in the frequency range up to 20 GHz with a high gain, are determined. The switching time delay is equal 0.81 ps at control voltages are equal 0.5 V.

The TCAD model of a half-adder is developed in the basis 2NAND. According to the simulation results, the efficiency of the prototype, which performs binary code addition operations with a delay of 4.2 ps at a supply voltage of 0.5 V and a frequency of 20 GHz, is shown. In this case, the active power is 0.66 μW, the static power is 21.5 pW.

The obtained results create a theoretical basis for the synthesis of low-voltage complex functional blocks with high performance and minimal occupied area, which meets modern requirements for digital applications.

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